COMPUTER AIDED DESIGN AND IMPLEMENTATION OF CONVERTER CIRCUITS APPLIED FOR PHOTOVOLTAIC SYSTEM

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ABSTRACT

This research intents to design and laboratory implementation of a power electronic converter, which is useful for home applications, industrial, communications, street light and water pumping using solar cell source. The design is based on a step up boost DC/DC converter followed by a full wave SPWM inverter. The nominal power rating is 1.25kW and can operate from any DC source such as DC battery besides fuel cells. The system which consists of the following stages (PV, converter, inverter, DC link, filter and snubber circuit), is designed primarily with a general module depending on Orcad PSPICE program to produce power output nearly 1.25kVA at 50Hz with a pure sinewave output for both voltage and current. After designing and simulating this system, the intended SPWM inverter are built experimentally to compare its results with the simulated one.

INTRODUCTION

The design of a photovoltaic (PV) system is generally addressed to the best matching between the energy supplied to the system by the sun, and the energy required by the load that is to be fed by the system. The ”best matching” can be searched in terms of minimum cost, best efficiency, reliability or a compromise between these constraints. Historically, photovoltaic systems have been used as powers supply only for special loads such as communication satellites. The continuous advances in the area of

semiconductor materials led to the development of commercial PV cells with competitive cost, as compared with conventional generating systems. As a result, PV cells are now prominent as an alternative energy source [1]. This paper presents the design and laboratory implementation of a power electronics converter. The converter is made up of a dc-dc step up boost structure and a voltage source inverter (VSI) with optimized sinusoidal pulse width modulation

(PWM) strategy. The converter uses MOSFET as power switches because it is the available device. The full bridge inverter configuration is frequently employed, wherein the power semiconductor switches can be controlled by a variety of PWM techniques (Boost and Ziogas), SPWM control strategies involving either unipolar or bipolar (Mohan) switching are quite common since the harmonics significant amplitude are pushed into the high frequency range near the carrier frequency [2].

The proposed system

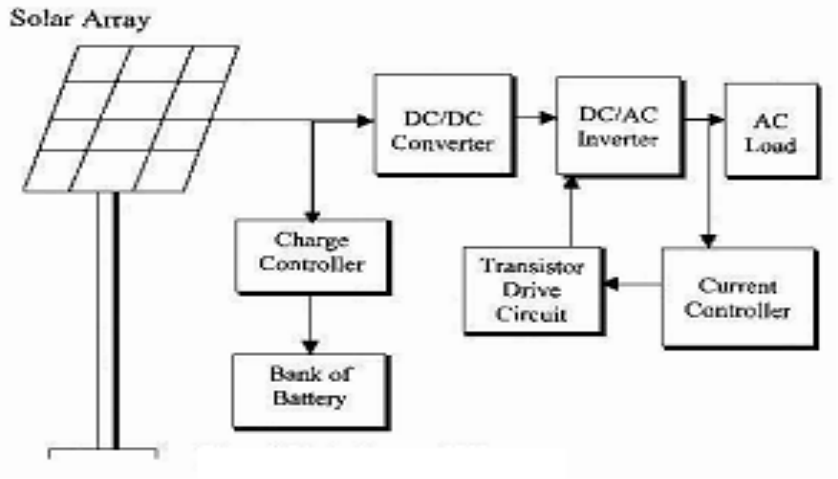

Figure 1: Block diagram of the PV system

Practical photovoltaic solar system designed with a power of 2kW is shown in fig.1. The analysis of the complete design circuit was carried out by using the PSPICE software. The PV arrays are current source so it is necessary to include a link capacitor between the array and the DC/AC inverter to obtain a voltage source in the input of the last one [3]. The step up boost converter operates in the continuous conduction mode. It has been designed for output voltage of 320V, switching frequency 2.5kHz, duty cycle .4 and 1.5kW. Figure 2 shows the boost stage as represented in PSPICE. Op1 and Op2 generate PWM as drive signal to the switching device (MOSFET – IRFP460).

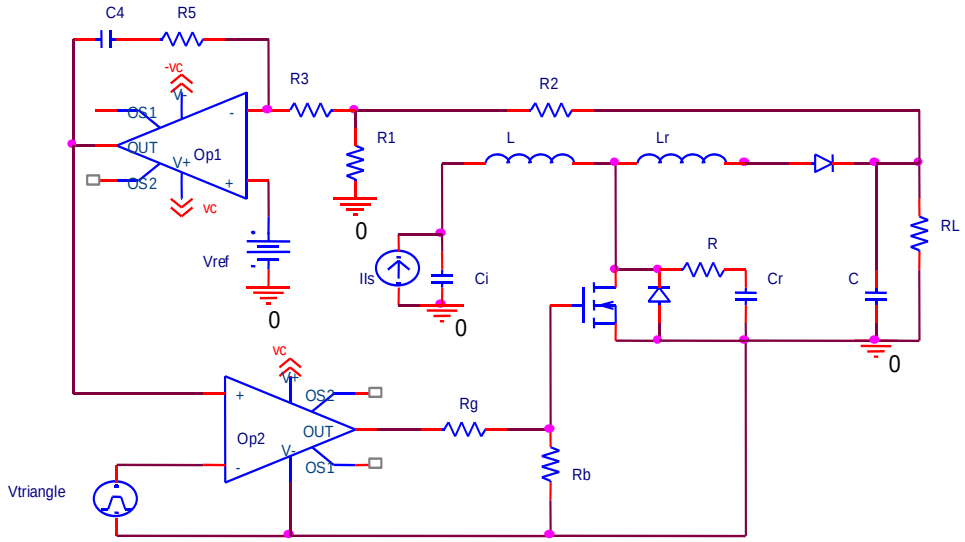

Figure 2: step-up Boost converter as represented in PSPICE

The output capacitor C for a boost stage is generally selected to limit the output ripple voltage to the required level by the specification. Its value was calculated according to the following formula [4]:

$$C \geq \frac{I_O(\max) \times D_{\max}}{f_S \times \Delta V_O} \quad (1)$$

Where:

I_o (max) is the maximum output current

D_{max} is the maximum duty cycle

The minimum value of inductor to maintain continuous conduction mode can be determined by the bellow formula [4]:

$$L_{\min} \geq \frac{Vo\ T_s}{16\, I_{o(crit)}} \quad (2)$$

$I_{o(crit)}$: the minimum output current to maintain continuous conduction mode. The complete structure of the full bridge inverter represented by PSPICE is shown in fig.3 where MOSFET (IRFP460) used as switching device and BYT30P-400 as free wheel diode, C_1, C_2, C_3 and C_4 are the resonant capacitors and act as snubbers circuit for the switches during turn off and limit the

across the switches[5]. dv/dt

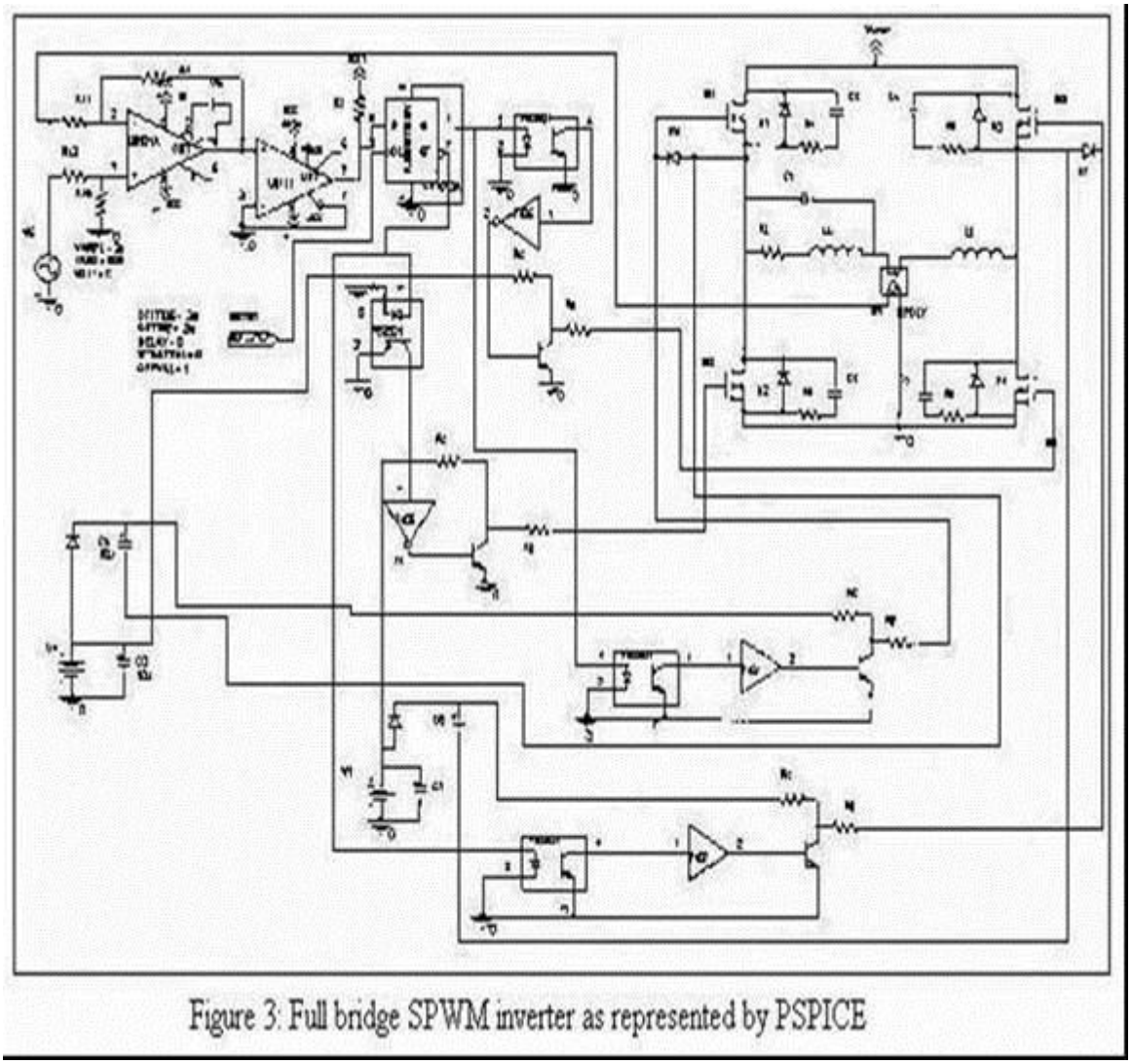

Figure 3: Full bridge SPWM inverter as represented by PSPICE

Other important parameter to consider for the power circuit design is the value of the output inductor L. The chosen value of this inductor must be a compromise between the maximum current rate at the converter output and low current ripple of the same signal. The maximum current rate happens when the sinusoidal waveform assumes a

null value. In this condition, the inductance value is determined by the input source as explained by equation (4). [6]

$$\left.\frac{di_o}{dt}\right|_{t=0} = 2\sqrt{2}\,\pi\, f_o\, I_{orms} \tag{3}$$

$$L_{\max} = E\,\frac{dt}{di_o} \tag{4}$$

This theoretical value of the inductance was chosen for an input voltage source of E=320V, f_o = 50Hz and I_{orms} = 3A. A slightly lower inductance value is adopted in the project. The results were as follows:

$$\left.\frac{di_o}{dt}\right|_{t=0} = 1332.18A/s \text{ and } L_{adopted} = 200mH$$

If a rear sinusoidal (AC) is required, a low pass filter (consisting of L and C) is connected at the inverter output terminals in order to minimize the harmonic distortion of the load voltage.[2]

The output PWM that is obtained by comparing the output current with a reference signal the difference than it is sampled by a sampling frequency. Signal is applied to the drive circuit through an opto-coupler, which acts as isolation stage between the PWM generator and power stage. The output of the opto-coupler is applied to a buffer stage IC (7406, 7407) that feeds the bases of the transistor with appropriate signal required to drive it. The transistor supplied pulse of sufficient voltages, and drove current to the gate of the switching device (MOSFET) through a resistance R_g.

H-Bridge configuration has another unique requirement, that is the upper (power switch's) emitter is not at the ground potential, but is floating, making it necessary to employ Boot-Strapping technique to drive the power switch[7]. The complete PV system (converter and inverter circuit) with PWM and gate drive circuit is shown in fig.4.

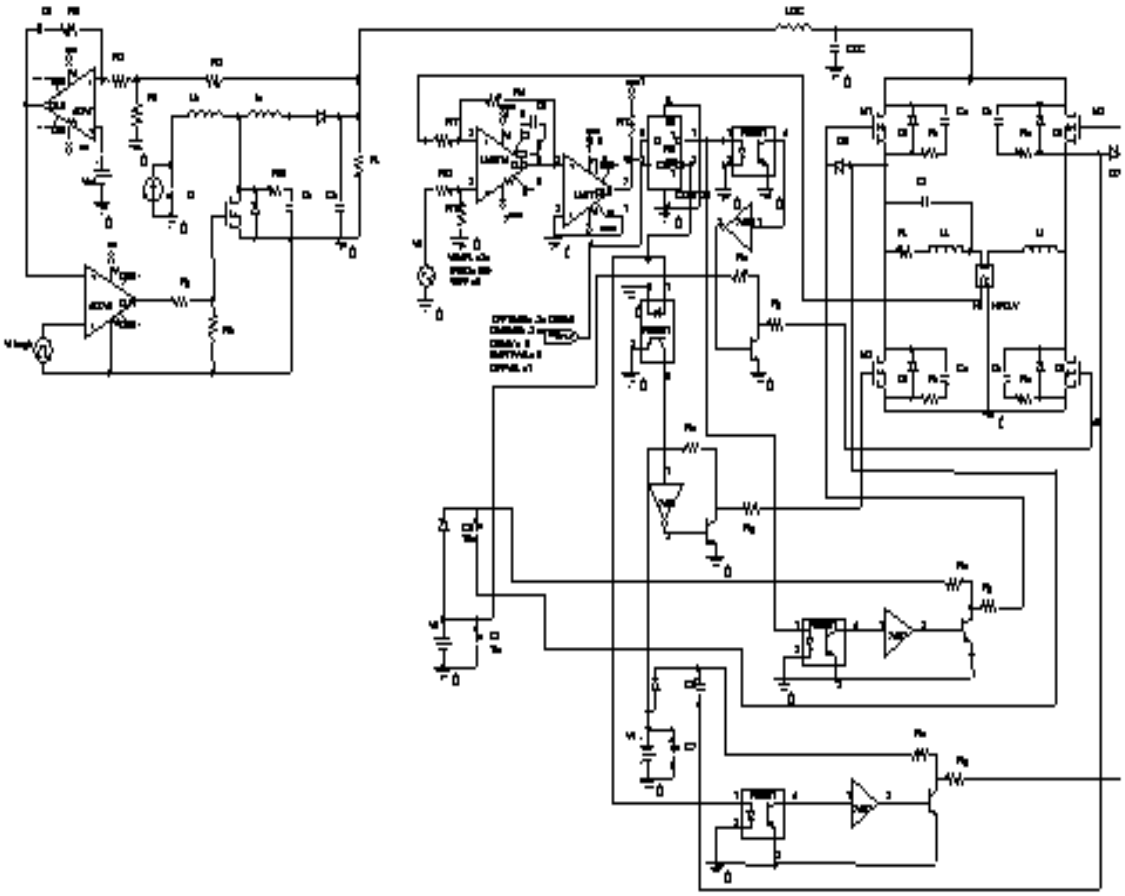

Figure 4: PV system as represented in PSPICE

RESULTS AND DISCUSSION

The PWM was implemented through experimental prototype. The parameters previously determined were used in the inverter at the sampling frequency f_c=2.5khz and output frequency f_o=50Hz. The circuit used is shown in fig.5. The pulse widths

and timing are defined using a program (supported to EPROM I.C 2716) that determines pulse requirements.

By generating a drive clock using programmable crystal oscillator (PXO600), a clock of frequency 30kHz is generated. The clock is applied to 12 bit binary counter. The outputs of the counter represent the addresses of the EPROM. The inverter performance was verified to an output active power of P_o = 1.25kVA

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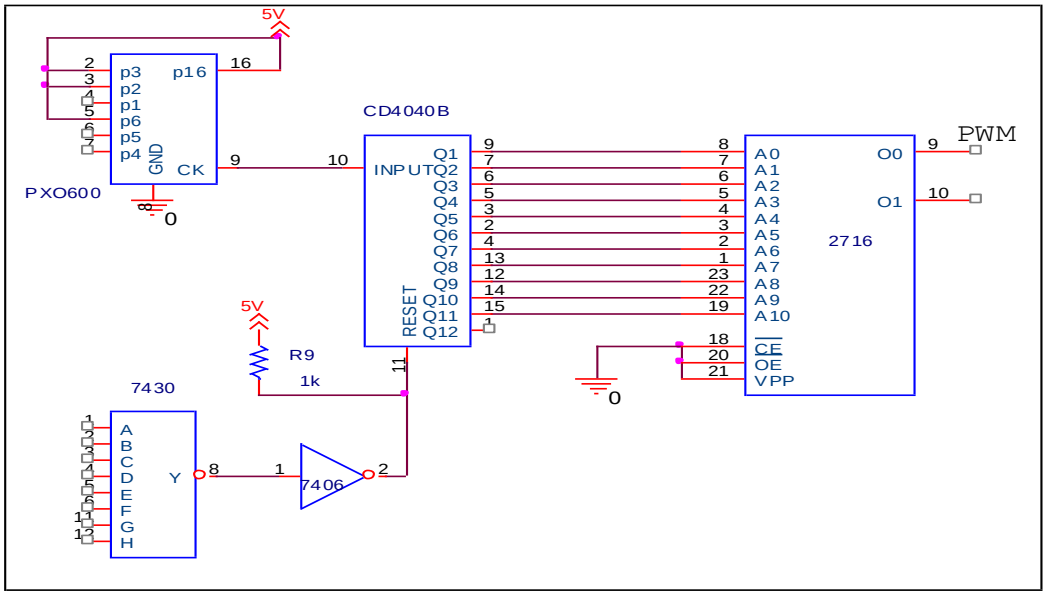

Figure 5: Pulse width modulation circuit that is used experimentally

Some experimental results are shown to demonstrate the performance of the system. Figure (6) depicts the signal at the gate of MOSFET (M_3) and MOSFET (M_4) which are shown in fig.(3). This figure explains the PWM signal, which is similar to that obtained in PSPICE simulation in number of pulses and pulse width.

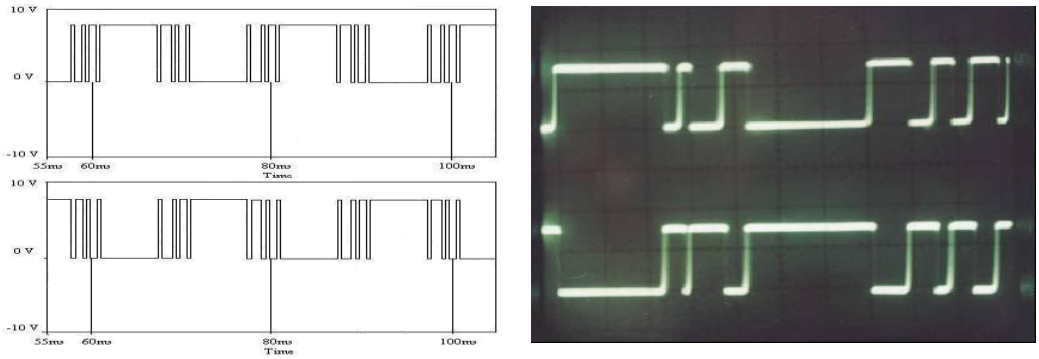

Figure 6: PWM signal from PSPICE and experimentally

Figure (7) represents the sinusoidal output current. This current have amplitude 2*2V/div divided by 1.Ω. Therefore, the rms value is equal to 3A. The scale of the time base is 5ms/div.

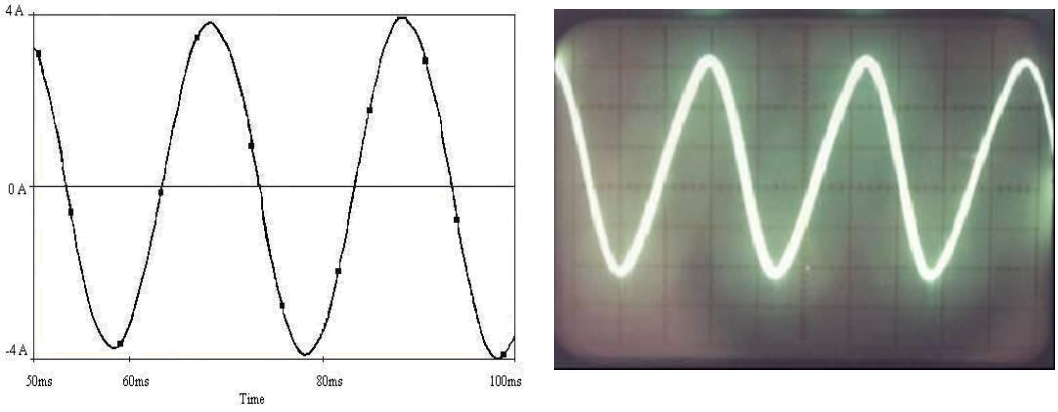

Figure 7: Output current from PSPICE and experimentally

Figure (8) shows the sinusoidal output voltage of amplitude 310V and the time base of this signal is 5ms/div. Also this signal is similar to that obtained in PSPICE.

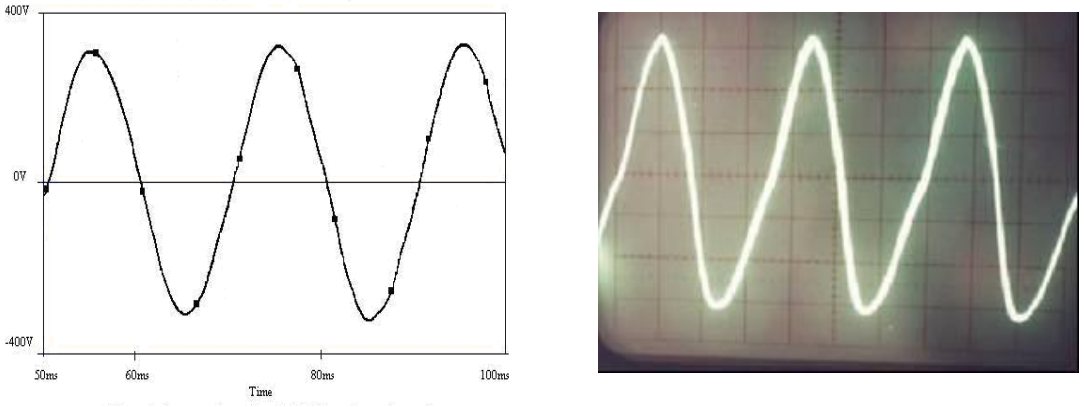

Figure 8: Output voltage from PSPICE and experimentally

In order to see the behavior of the output voltage against the frequency, fig.9 shows the maximum voltage appeared at 50 Hz. The behavior of the output current against the frequency is shown in fig.10. The peak at 50Hz has a value of about 3A; peaks at 150Hz, 250Hz and 350Hz (the 3^{rd} 5^{th} and 7^{th} harmonic) have a value of about 80mA, 30mA, 25mA that is 2.6%, 1%, 0.8% of the fundamental harmonic.

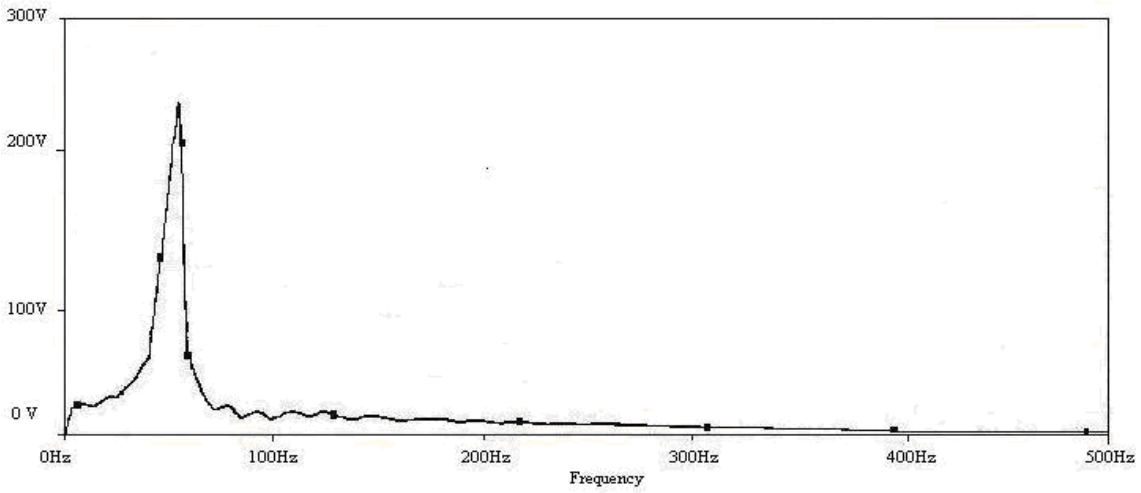

Figure 9: Harmonic distrtion spectrum for voltage

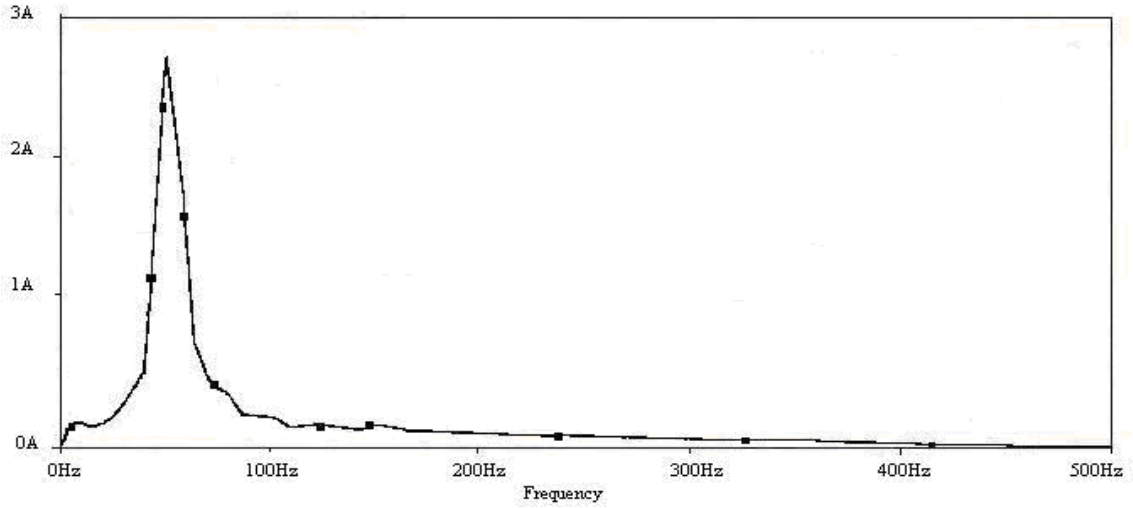

Figure 10: Harmonic distortion specturm for current

CONCLUSION

The proposed PV system circuit has been simulated with standard software (PSPICE) available and the results obtain has been compared with practical results, like the efficiency of the PV system, which is built on the laboratory, was about 93% and the result obtained from PSPICE simulation about 92% and this is agree with the efficiency obtain experimentally as well as the harmonic distortion spectrum for both the current and voltage was very low (lower than 3%).

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