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DESIGN AND IMPLEMENTATION OF A DIGITAL PHASE LOCKED LOOP FREQUENCY SYNTHESIZER IN THE L BAND

Nasser N. Khamiss Al- Ani
College of Informatics Technology,
Al-Nahrian University

Walid A. Mahmoud **Eng. Riadh A.Mahdy**
College of Engineering, Baghdad University

ABSTRACT

This paper proposes a design and implementation method of DPLL frequency synthesizer system. Such a system offers many advantages such as minimum complex architecture, low power consumption, and a maximum use of large scale integration technology. It can be used in many applications as cordless telephones, mobile radios and other wireless products. A (2.4 – 3.6) GHz frequency range is designed and implemented with a 100KHz frequency step size. A spurious output levels of -70 dBc, an output power should be greater than 10 dBm, and a phase noise less then (-100) dBc/Hz at 100 kHz offset from the carrier are considered in our design. The channel selection is guided by digital gating circuits with thumbwheel switches. An option of FM modulation of 5 MHz FM bandwidth is also included.

الخلاصة

هذه الورقة تتناول تصميم وبناء مركب ترددات في حزمة "L" لحل بعض المشاكل المتعلقة بمنظومات الاتصالات. المطلوب تصميم مركب ترددات يغطي الحزمة (2.4–3.6) GHz وبسعة قفزة 1 MHz . سعة الإشارة الغير مرغوبة -70dBc ، مع قدرة خرج أكبر من 10dBm ، وضوضاء طورية أقل من (-100) dBc/Hz عند تردد انحراف 100 kHz . تغير الترددات أو إختيارها يتم عن طريق دوائر الكترونية رقمية بإستخدام مفاتيح خارجية . ضمن التصميم تم اختيار تحميل نوع FM بعرض حزمة تتجاوز الـ 5 MHz . تم تطبيق تقنية القفز الطوري الرقمي الجزئي لإنجاز هذا التصميم . أستُخدمت مواد ذات تقنيات متطورة وصغيرة الحجم في عملية البناء . حيث أستُخدم مذبذب (VCO) ومقسمات تردد من نوع المكونات معتلية السطوح (SMT)، ومكبرات إشارة راديوية 50Ω صغيرة الحجم . قُيست المنظومة فوجدت بأنها تغطي المواصفات المطلوبة من حيث سعة القفزة والضوضاء الطورية والإشارة الغير مرغوب بها والقدرة الخارجية .

KEY WORDS
Frequency synthesizer, digital phased locked loop.

INTRODUCTION

A Phase Locked Loop (PLL) is an electronic system, which synchronizes an internal controlled oscillator, in frequency and phase, with an external input signal. More precisely, the PLL is a servo system, which controls the phase of its output signal in such a way that the phase error between output phase and reference phase to a minimum while output signal frequency is the same as input one. The input/output signal can either be sine wave or square wave. The PLL can be used as a frequency synthesizer by placing a loop divider (frequency divider) in the feedback path [Gursharan Reehal 5, Juhn Salvey and Stephanos Thompoulos, 1997].

The system design can be achieved as an integer N frequency synthesizer or as a fractional-N frequency synthesizer. The integer N system introduces many limitations as a large divide ratio, a small reference frequency, and a small loop bandwidth. While the fractional-N frequency synthesizer overcomes the above limitations and introduces many advantages as, almost arbitrary frequency resolution, fast frequency switching speed, less phase noise caused by VCO, and small divide ratio, less phase noise [Samuel Michael Palermo, 1999].

Principle disadvantage of fractional-N frequency synthesizer is spurious outputs, which are caused by the periodic change in the divide ratio.

SYSTEM DESIGN AND IMPLEMENTATION

This paper deals with a design of a fractional N digital phase locked loop synthesizer corresponding to the given requirements. The synthesizer is designed and implemented according to the required specifications by using a new technology with high quality and mini-size components; where it uses a mini-size VCO, Surface Mount Devices Technology (SMT) of 8 pins prescalers, SMT 50Ω mini-size amplifier, SMT mini-size chip resistors and chip capacitors. All these components with a frequency range up to 4 GHz. The proposed system is given in **Fig. (1)** which consists of; voltage controlled oscillator VCO, prescaler divides by 4 at (4)GHZ range, dual modulus prescaler divides by 64/65 at 1GHz range, wide band power amplifier at 4GHZ range, programmable frequency divider, Crystal oscillator as a reference oscillator, phase/frequency detector and lock detect circuit, loop filter, suppression filter, and channels lookup table circuits and thumbwheel switches.

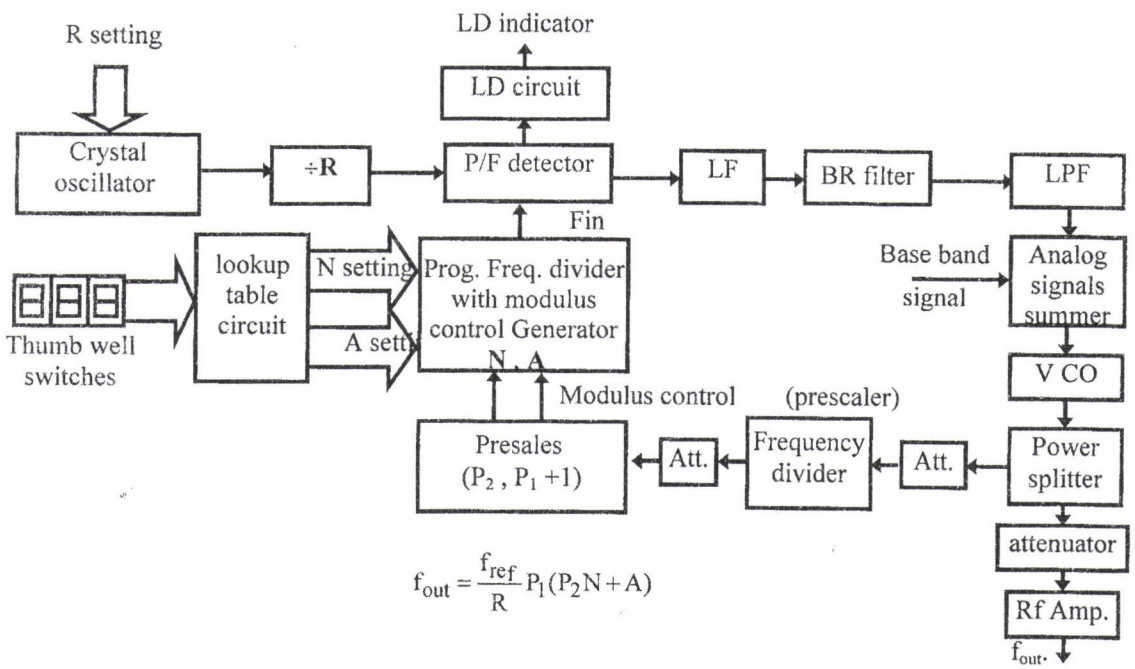


Fig.(1). System block diagram

Voltage Controlled Oscillator (VCO)

The voltage-controlled oscillator used in the system is an 8 pins metal package and has the following Characteristics of : Frequency range of 2100-4000 MHz, output power of 10 dBm, tune voltage of (1-20) V, tuning sensitivity of (30-50) MHz/V, power supply of 8V and 30 mA, SSB phase noise at 1KHZ offset of (-70) dBc/Hz, at 10 kHz offset (-95) dBc/Hz, at 100 kHz offset (-115)dBc/Hz, and 1 kHz offset (-135) dBc/Hz [Mini Circuit, 2000].

Fig. (2) shows a VCO test circuit. A measurement of the frequency

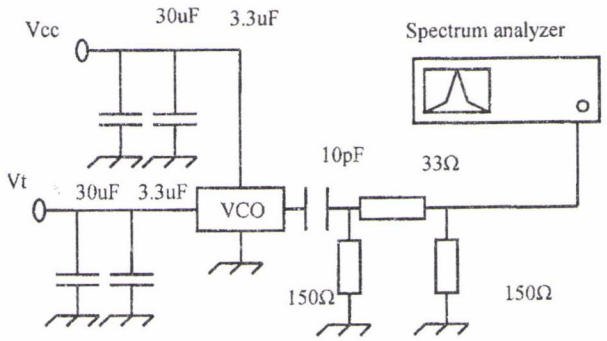


Fig.(2). The VCO phase noise and spurious measurement circuit

spectrum of the VCO at 2700 MHz is achieved by using the circuit in **Fig. (3).**

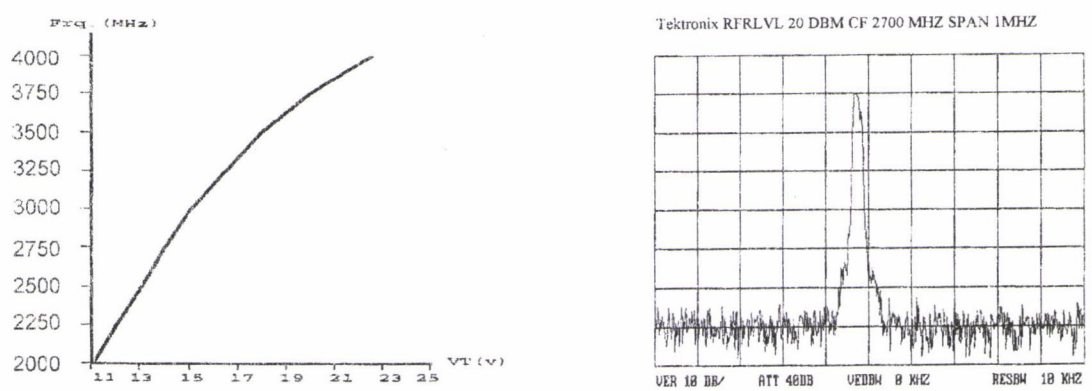
The phase noise can be measured by using the spectrum analyzer corresponding to the following relationship:

Phase noise = [(N-S) dB -10 log (RB) HZ] dBc / Hz (1)

Where N is a noise power at frequency offset in dBm, S is a signal power in dBm, RB is a resolution bandwidth in Hz [Manassewitsch V. 10].

The spurious level can be measured as follow:

Spurious level = (spurious signal power-signal power) dBc (2)



(a) (b)

Fig.(3 a) VCO characteristics, b) spectrum of VCO at 1900 MHz

Phase Frequency Detector: (PFD)

A PD circuit is shown in **Fig. (4),** which is available in several versions as a single chip (IC). It provides an indication of frequency error when the loop is out of lock, so it is called a phase-frequency detector (PFD) [Gardner F. M, 1979].

The PFD has two output terminals, labeled ϕR and ϕV. The low (pulled down) condition is active while the high condition is inactive on each terminal. Both ϕR and ϕV can be high simultaneously, but not low. **Fig. (5)** shows duty ratio of PFD. The timing diagram of PFD is shown in **Fig. (6),** where d_R and d_V are the duty ratio of ϕR and ϕV outputs respectively, θd is a phase difference between f_R and f_V. It can be seen that the active phase range is $=360^{\circ}$(MOTOROLA1995, Dhafer R.Zaghar1997).

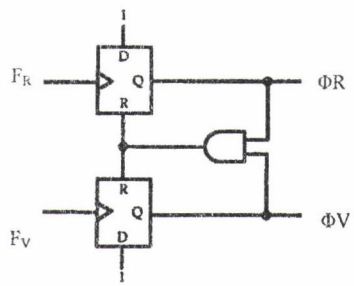


Fig. (4) Phase- frequency detector

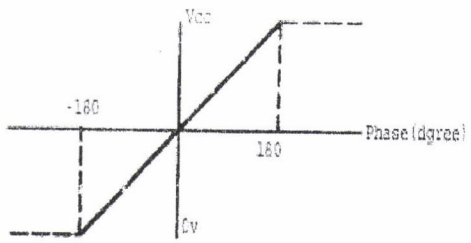


Fig. (5) Duty ratio of phase-frequency detector

The phase detector conversion gain ($K\phi$) can be found from **Fig. (5)** as follows:

$$K\phi = \frac{\Delta Vout}{\Delta \phi in} = \frac{5V - 0V}{2\pi} = \frac{5(V)}{2\pi(rad)} V/rad \quad (3)$$

Where: ΔVout is the peak PFD voltage change = power supply voltage (5V). While $\Delta\phi$in is the input phase difference in radians, it is a 2π not 4π, because one part of PFD is active according the error.

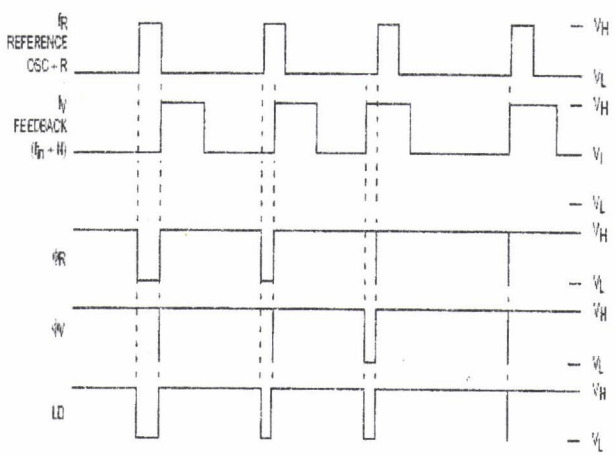


Fig.(6) Timing diagram of PFD

Prescalers

There are two used prescalers in the system, as shown in **Fig.(7).** The first prescaler is a divider by four, used up to (4) GHz frequency range. It is an eight pins plastic package (SMT) device.
Second prescaler is a dual modulus divide by (64/65) divider, up to a 1GHz frequency range; it is an eight pins plastic package SMT device. It has an external control called modulus control (MC) to select the division ratio 64 or 65, this control signal is generated by swallow counter to make the synthesizer in a fractional mode.

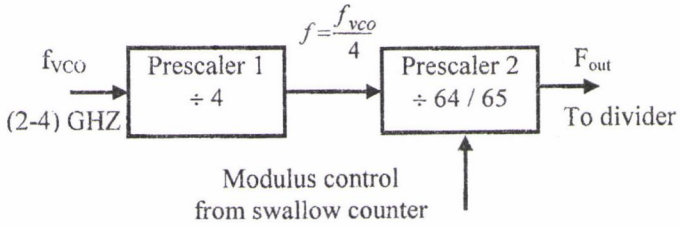


Fig.(7) Prescaler connection

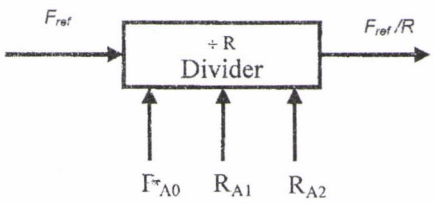


Fig.(8) Reference frequency divider

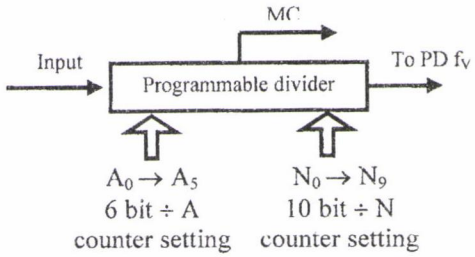


Fig.(9) Programmable Divider

Programmable Dividers and Swallow Counter

There are two programmable dividers in the system, see **Fig. (1):**

Reference Frequency Divider (R divider)

It is a selectable divider of eight possible division ratios. **Fig.(8)** shows its configuration, where R_{A0}, R_{A1}, R_{A2} are an address code to select the division ratio as detailed in **Table (1).** There is a possibility of using maximum input frequency up to 20 MHz with this type of divider [MOTOROLA9, Asmaa Numan Mahir 1994].

Table (1) possible division ratios

Address Code			Division ratio
R_{A2}	R_{A1}	R_{A0}	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

The N and A Programmable Dividers with Modulus Control (MC) Generation

This part uses the output of second prescalers to divide it by a programmed ratio, see **Fig. (9).** The output of this part feeds the phase detector to compare with reference frequency, and then generates the error signal.

Modulus control signal is generated to control the division ratio of second prescaler (P_2) to generate a fractional mode action. N address provides the data is preseted into ÷N counter when it reaches the count of zero. An address defines the number of clock cycles of input frequency that require logic zero on the modulus control output. This divider generate MC as following, see **Fig. (10):**

a- At starting MC = 0, prescaler ratio = P_2+1 = 65, and (÷A) counter will begin to count from (0) to $(9A)_H$.

b- When (÷A) counter become 0, MC become 1, second prescaler division ratio is P_2 = 64, and this case remains still until (÷N) counter is counting the rest (N-A).

c- After (÷N) counter counts the rest (N-A), MC will become 0 and ÷A counter will start to count from 0 to A again and the operation is repeated periodically, [MOTOROLA1995].

Now it can be derive the formula of the input frequency (f_1) in terms of output frequency (f_3) and division ratio P_2, N, and A as follow; see **Fig. (15):**

$$f_2 = Nf_3 \tag{4}$$

$$\left.\begin{aligned} f_1 &= p_2 f_2 \quad , when\ MC = 1 \\ &= (p_2 + 1) f_2 \quad , when\ MC = 0 \end{aligned}\right\} \tag{5}$$

It can be found (f_1) by averaging two cases of equation (5) as follow:

$$\left.\begin{aligned} f_1 &= f_2 p_2 \frac{N-A}{N} + f_2 (p_2 + 1)\frac{A}{N} \\ &= f_2 p_2 - \frac{f_2 p_2 A}{N} + \frac{f_2 p_2 A}{N} + f_2 \frac{A}{N} \\ &= \frac{f_2}{N}(Np_2 + A) \end{aligned}\right\} \tag{6}$$

Substitute equation (4) in equation (6),

$$\left.\begin{aligned} f_1 &= f_3 (Np_2 + A) \\ A &\lhd N, A \le p_2 - 1 \end{aligned}\right\} \tag{7}$$

From equation (7), it is clear that N represents an integer part of P_2 and A is a fractional part of P_2.

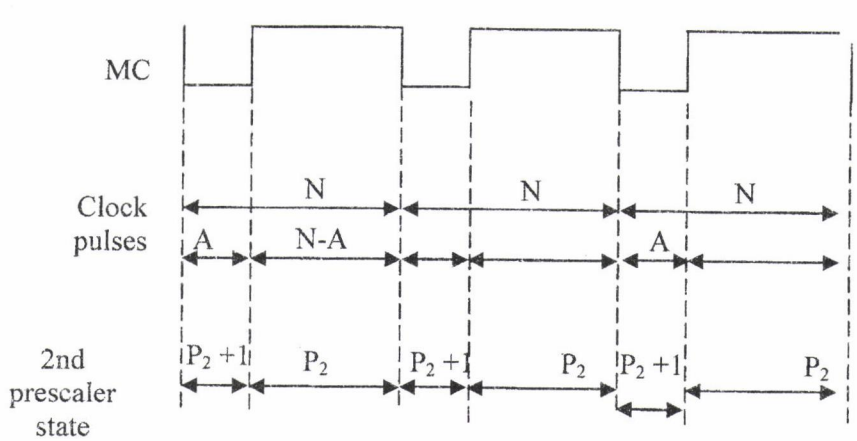


Fig.(10) Modulus control generation timing diagram.

Reference Oscillator

In order to provide a stable reference frequency, a crystal oscillator must be used. A fundamental mode crystal of parallel resonant at the desired operation frequency is connected as in **Fig.(11),** which is defined as a pierce crystal oscillator.

A crystal characteristic of 4MHz frequency, tolerance at 25 C°of 20 parts per million (PPM), Temperature stability of 50 PPM, and load capacitance of 30 pF is used in the oscillator. In our application don't need a very low tolerance and high temperature stability crystal oscillator. There are guide lines that provide a reasonable compromise between IC capacitance, IC input/output capacitance, and crystal shunt load capacitance (C_L).

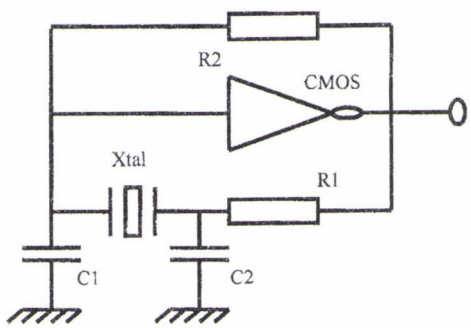


Fig.(11) CMOS pierce crystal

Loop Filter

Active filter in **Fig.(12)** is used as a loop filter where it provides a better tracking performance [QUALCOMM ASIC PRODUCT 1985].

The phase detector outputs are high frequency large amplitude pulse signals, these pulses on the input of loop filter op-amp can cause nonlinear saturation in the amplifier. One solution is to pre–filter the error pulses before they reach the active filter by inserting an RC low pass section by splitting R_1.

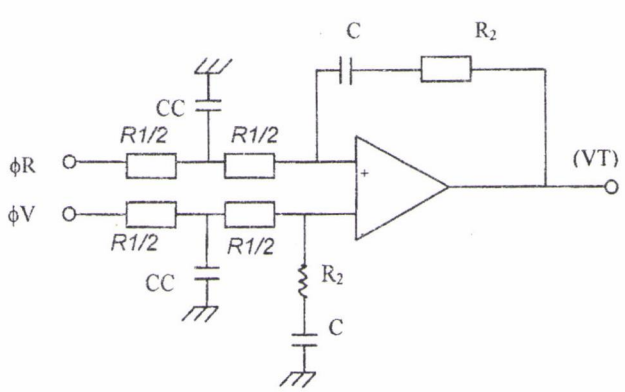


Fig. (12) Loop filter circuit diagram

Suppression Filter

The suppression filter consists of a band reject filter followed by a low pass filter, see **Fig.(13).** The band reject filter is used to reject the reference frequency $f\phi$. While the low pass filter is used to reject the harmonics of $f\phi$.

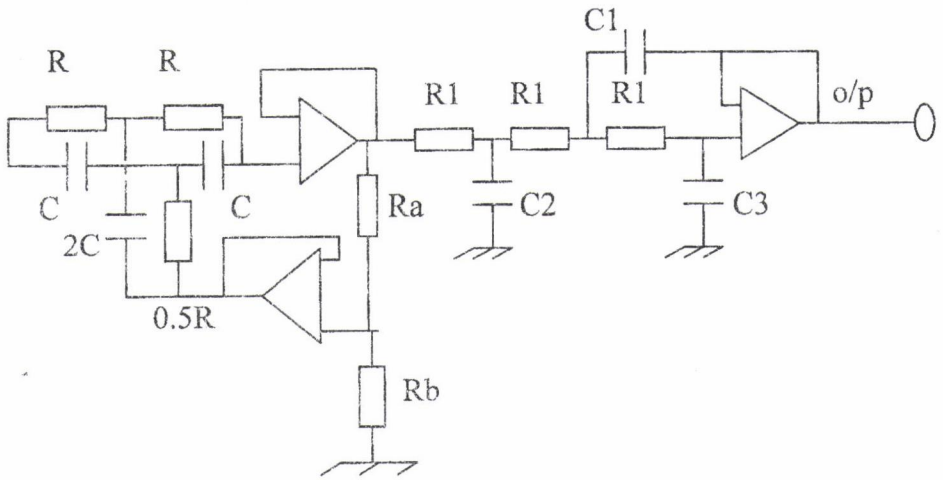


Fig.(13) circuit diagram of suppression filter

Type of band reject filter is a twin–T with positive feed back; **Fig.(14)** shows its frequency response.

Channels Lookup Table Circuit and Thumbwheel Switches

A three thumbwheel switches connected with a two 16k byte EPROM's are used, see **Fig.(1).** The thumb well switches select the number of channel from 0 to 399, i.e. frequency from 2.4-to-3.6 MHz with 1 MHz step size. The EPROM's is used as a lookup table to convert the code of thumb well switches to the binary code of programmable frequency dividers.

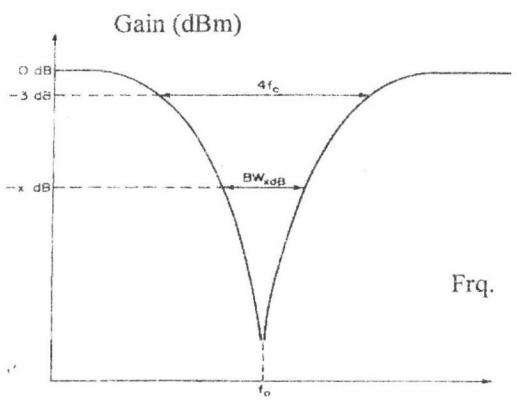


Fig. (14) Freq. response of twin T filter, [Arther Williams 1988].

Power Amplifier

A 50Ω input/output impedance, (SMT) miniature amplifier covering the DC to 4 GHZ frequency range with up to (10) dBm typical output power is used in the system. **Fig.(15)** shows the power amplifier and the connection.

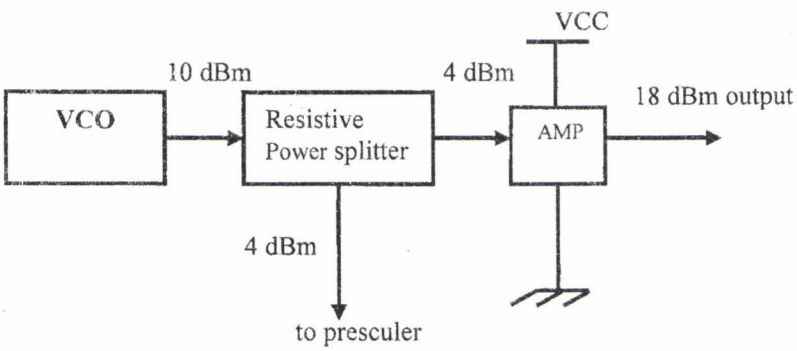


Fig. (15) Power Amplifier

TEST AND MEASUREMENTS

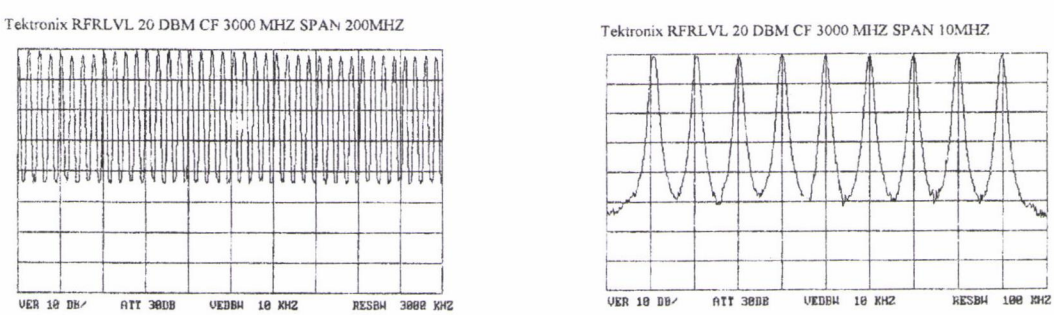
In this section will test the performance of the system with respect to the design specification such as frequency range, minimum step size, phase noise, spurious output, output power, power fluctuation versus frequency, and FM modulation. A spectrum analyzer used to measure the frequency domain measurements, and oscilloscope used to measure the time domain measurements, function generator used to feed the base band signal to the part of FM modulation in the synthesizer. A GPIB bus is used through a PC to store the results.

Frequency Range and Step Size

The synthesizer must be covered a range of frequencies from 2.4 GHZ to 3.6 GHZ with step size 1 MHz. **Fig. (16a)** shows frequencies (2-4) GHZ with step size 10 MHz, and **Fig. (16b)** shows frequencies from 3950 MHz to 3050 MHz with step size 1 MHz.

Spurious Outputs Measurements

It will be choose frequencies (2700, 2900, 3100) MHz as samples to measure the spurious outputs and phase noise. **Fig. (17)** shows the spectrum of different six cases, **Table (3)** shows the spurious values of these cases.



(a) (b)

Fig. (16) synthesizer output spectrum

Phase Noise Measurement

The phase noise will be measured as a single side band (SSB) phase noise according to equation (1):

(Phase noise) $_{SSB}$ = [(noise power at offset – signal power) dB
–10 log (resolution bandwidth) HZ] dBC / Hz.

Table (4) shows the phase noise measurement of different six cases from the synthesized. **Fig. (18)** shows spectrum of the fifth case.

Frequency Stability with Temperature

This feature is measured at different frequencies. Using a heat gun to increase the temperature of the synthesizer and a digital temperature meter to measure the temperature variation. The frequency variation is measured by using spectrum analyzer.

The temperature frequency depending on the temperature stability of crystal oscillator that used as a reference oscillator, where the stability at any frequency can be found as follows:

$$\max.frequency\ drift\ at(f) = f(MHz) \times crystal\ stability(PPm)Hz \qquad (8)$$

The crystal that used in reference oscillator has a 50 PPM temperature stability therefore the maximum drift at 3100 MHz due to temperature effect is:

$$\max.drift\ r\ at\ 3100MHZ = 3100 \times 50 = 155KHZ.$$

Output Power and Power Fluctuation Versus Frequency

The output power must be at least 10 dBm with fluctuation less then 3dB. **Fig.(16)** shows the power variation with respect the frequency.

FM Modulation

Fig.(19) shows FM modulation spectrum with different output frequency and same base-band (335 kHz). It can be seen that the FM bandwidth of the three cases is not completely similar, because the VCO is not completely linear around the frequency band [Paul H.Young 1985, Hayward W.H. 1982].

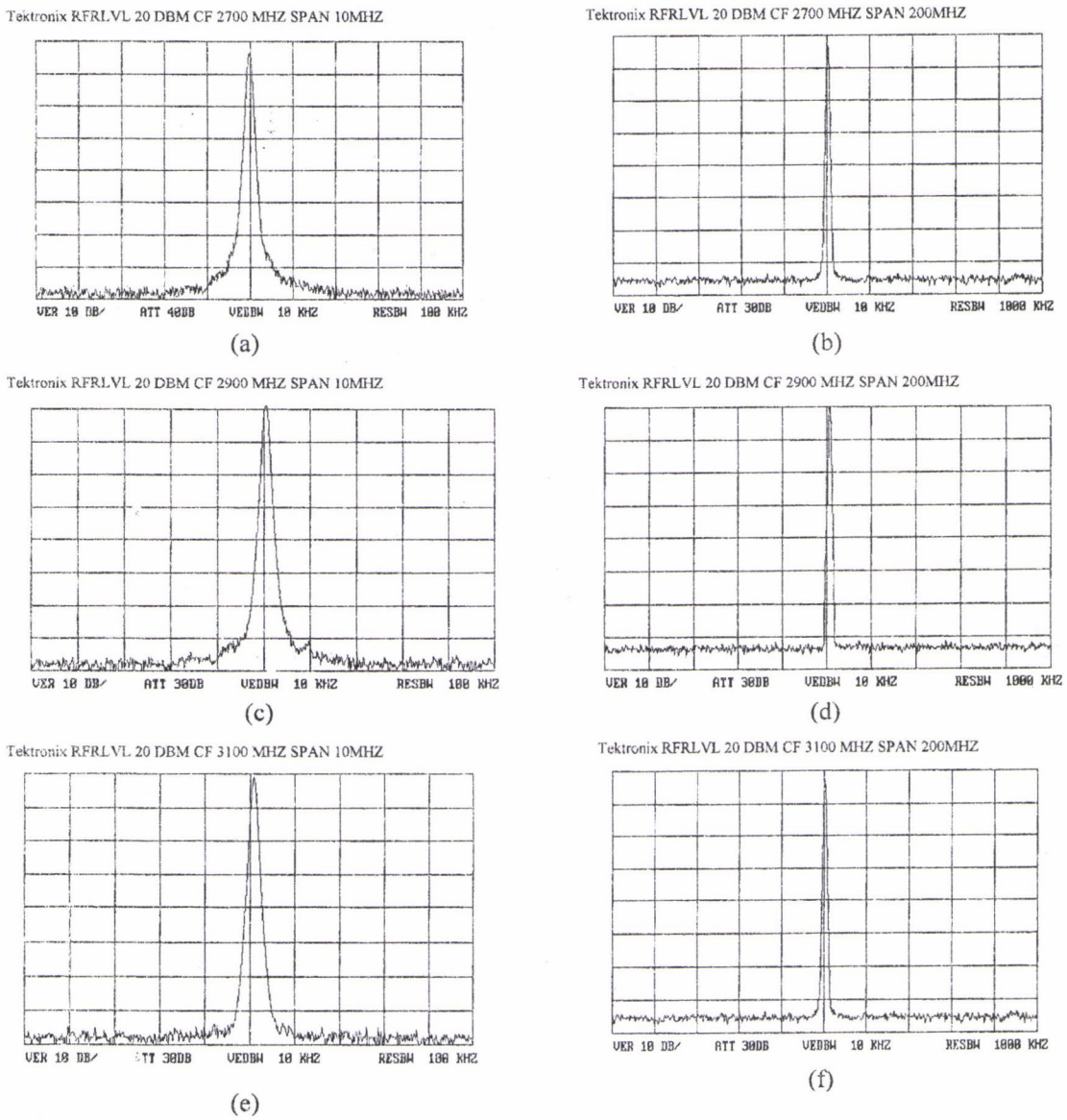


Fig. (17) Spurious outputs corresponding to the measured frequency (center frequency)

Table (3) spurious outputs measurement

Case	Spurious (-dBC)
f_C = 2700 MHz, span = 10 MHz	72
f_C = 2700 MHz, span = 200 MHz	72
f_C = 2900 MHz, span = 10 MHz	71
f_C = 2900 MHz, span = 200 MHz	74
f_C = 3100 MHz, span = 10 MHz	74
f_C = 3100 MHz, span = 200 MHz	72

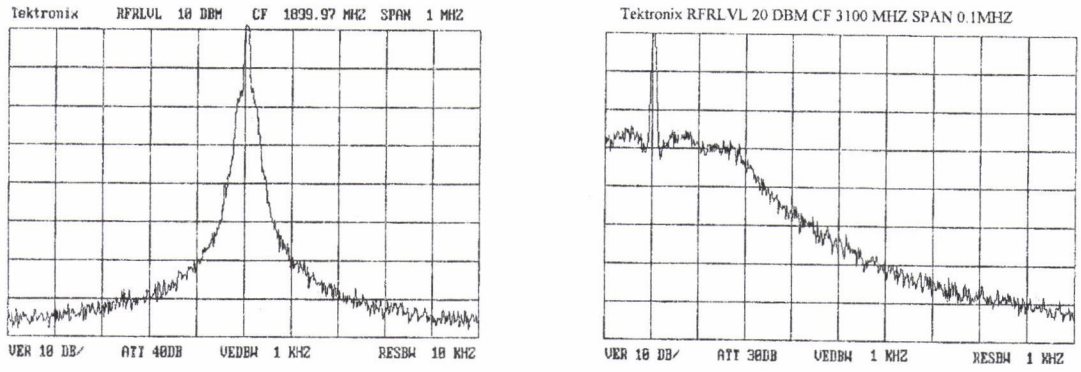


Fig. (18) Phase noise at synthesized frequency Fs=3100 of a span=1MHz (left) and a span of 0.1 MHz (right)

Table (4) phase noise measurements.

	SSB phase noise in – dBC / HZ			
Measured frequency	f_{offset} = 1 kHz	f_{offset} = 10KHZ	f_{offset} = 100 kHz	f_{offset} =.5 MHz
f_S = 2700 MHZ	40	53	103	120
f_S = 2900 MHZ	43	58	105	117
f_S = 3100 MHZ	40	60	108	116

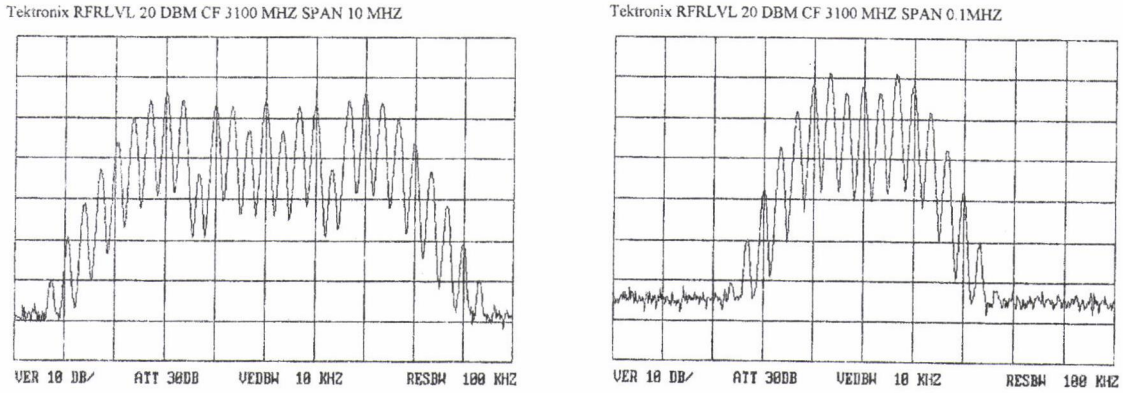


Fig. (19) FM modulation at frequency 3100 MHz of BW_{FM}=6.7MHz (left) and BW_{FM}=4.0MHz (right)

CONCLUSIONS

The implemented synthesizer is a single loop fractional (N) digital phase locked loop one. It is designed to cover (2.4-3.6) GHZ frequency band with 1 MHz frequency step size. The measurements show results of spurious outputs less than -70 dBc, a phase noise less than -100 dBc/HZ at 100 kHz offset from carrier, output power is 10 dBm, and this provides FM modulation facility of more than 5MHz bandwidth. Thumb wheel switches on front panel used to select the

frequency. It provides the typical solution for the given requirements. In the same time, it is inexpensive, save hardware and provides good spurious suppression and low power consumption. The results show that the phase noise is improved inspect of the noise due to the phase detector, dividers, op amps, filters, and when the multiplication ratio is high.

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